IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Shinji Ohuchi — Group Art Unit: 2814

Serial No.: 10/800,693 — Examiner: M. Pizarro-Crespo

Filed: March 16, 2004 — Confirm. No.: 1770

For: SEMICONDUCTOR DEVICE INCLUDING A PROTECTIVE BACKING RESIN LAYER

REQUEST FOR RECONSIDERATION

U.S. Patent and Trademark Office
****Via efiling****
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Date: December 30, 2008

Sir:

In response to the Office Action dated September 4, 2008, the period for response having been extended one (1) month to January 4, 2009, the following remarks are respectfully submitted in connection with the above-identified application.

Remarks/Arguments begin on page 2 of this paper.

REMARKS

Claims 12, 15-17, 20-22, 25-27, 30 and 31 are pending in the present application.

Claim Rejections – 35 U.S.C. 112, First Paragraph

Claims 12, 15-17, 20-22, 25-27, 30 and 31 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. The Examiner has alleged that a protective layer made of a polymide resin being a UV-sensitive tape comprised of a hardened synthetic resin that bonds the UV-sensitive tape to a second surface of a semiconductor element is not described in the specification in such a way as to reasonably convey that Applicant had possession of the claimed invention. This rejection is respectfully traversed for the following reasons.

With reference to the present application as published (U.S. Patent Application Publication No. 2004/0173895), paragraph [0021] sets forth: ***"The protective tape 22, which is constituted of a hardened synthetic resin achieving a bonding function such as polymide or an epoxy resin, protects the rear surfaces of the semiconductor elements 10, which are constituted of a fragile material".*** Protective tape 22 is shown in Fig. 1 of the present application.

As further described in paragraph [0034] of the present application as published, with respect to Fig. 3(d): ***"the protective tape 22 is first peeled from the rear surface***

of the wafer through UV (ultraviolet ray) irradiation and then the rear surface is polished".

Accordingly, as should be readily understood in view of paragraphs [0021] and [0034] of the present application as published, protective tape 22 is indeed described in the specification as constituted of a hardened synthetic resin achieving a bonding function such as polymide resin, and that this protective tape 22 is peeled from the rear surface of the wafer through UV irradiation. The present application thus clearly supports a protective layer made of a polymide resin that is a UV sensitive tape comprised of a hardened synthetic resin bonded to a second surface of a semiconductor element, to the extent necessary to show that Applicant had possession of the claimed invention. Applicant therefore respectfully submits that the specification complies with the written description requirement, and that claims 12, 15-17, 20-22, 25-27, 30 and 31 are in compliance with 35 U.S.C. 112, first paragraph. The Examiner is therefore respectfully requested to withdraw this rejection.

Claim Rejections – 35 U.S.C. 102/103

Claims 12, 15, 17, 20, 22, 25, 27, and 30 have been rejected under 35 U.S.C. 103(a) as being obvious over the Elenius et al. reference (U.S. Patent No. 6,441,487) in view of the Hashimoto reference (WO 98-25297), the Kim et al. reference (U.S. Patent No. 6,187,615) and the Yamada reference (U.S. Patent No. 6,048,749). This rejection is traversed for the following reasons.

It is noted that the Examiner has relied upon the non-English language Hashimoto reference (WO 98-25297), specifically page 12, lines 21-28, as indicated at the bottom of page 5 of the current Office Action dated September 4, 2008. However, the Hashimoto reference has been provided and relied upon by the Examiner as including merely an English language abstract. An English translation of the reference has not been provided or relied upon by the Examiner.

As set forth in Manual of Patent Examining Procedure (MPEP) section 706.02, when an abstract is used to support a rejection, the evidence relied upon is the facts contained in the abstract, not additional facts that may be contained in the underlying full text document. Citation of and reliance upon an abstract without citation of and reliance upon the underlying scientific document is generally inappropriate where both the abstract and the underlying document are prior art. See *Ex parte Jones*, 62 USPQ2d 1206, 1208 (Bd. Pat. App. & Inter. 2001) (unpublished).

As further set forth in MPEP section 706.02: ***"If the document is in a language other than English and the examiner seeks to rely on that document, a translation must be obtained so that the record is clear as to the precise facts the examiner is relying upon in support of the rejection".***

Applicant respectfully submits that the Examiner's specific reliance upon the non-English language Hashimoto reference (WO 98-25297) in support of this rejection is improper in view of MPEP section 706.02. The Examiner has made specific reference to page 12, lines 21-28 of the non-English language Hashimoto reference in support of

the current prior art rejection. However, the content of the non-English language Hashimoto reference is not clear, and thus the record as to the precise facts the Examiner is relying upon in support of this rejection is unclear.

Accordingly, if this rejection is to be maintained, the Examiner is respectfully requested to provide, make reference to, and cite of record either an English language translation of the non-English Hashimoto reference (WO 98-25297), or provide and cite of record a non-English language equivalent of the Hashimoto reference, in compliance with MPEP section 706.02.

The semiconductor device of claim 12 includes in combination among other features a protective layer "made of polymide resin on the second surface of the semiconductor element,... wherein the protective layer is a peelably removable UV sensitive tape comprised of a hardened synthetic resin that bonds the tape to the second surface of the semiconductor element". Applicant respectfully submits that claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

As noted above, the semiconductor device of claim 12 includes a protective layer that is peelably removable UV sensitive tape, that is made of polymide resin and that is on the second surface of the semiconductor element. The second surface of the semiconductor element is opposite the first surface of the semiconductor element, wherein the first surface of the semiconductor element has an electrode, a wiring portion, a conductive post, a resin layer and an external connection thereon. The

protective layer of claim 12 that is peelably removable UV sensitive tape, that is made of polymide resin and that is on the second surface of the semiconductor element, inhibits reflex of the semiconductor element.

The primarily relied upon Elenius et al. reference as shown in Fig. 2 includes an organic protective coating 34 on the rear surface 16 of wafer 14. The primarily relied upon Elenius et al. reference does not disclose a protective layer that is a peelably removable UV sensitive tape on a second surface of a semiconductor element, as would be necessary to meet the features of claim 12. The Elenius et al. reference does not inhibit reflex of semiconductor wafer 14.

The Examiner has secondarily relied upon Fig. 10 and page 12, lines 21-28 of the non-English language Hashimoto reference (WO 98-25297). However, since the Hashimoto reference as relied upon is a non-English document, the record with respect to the facts relied upon by the Examiner in support of this rejection is unclear. This rejection is thus improper.

U.S. Patent No. 6,475,896 would appear to be an English language equivalent of the non-English language Hashimoto reference (WO 98-25297) relied upon by the Examiner. However, the Hashimoto Patent does not disclose a protective layer that is peelably removable UV sensitive tape made of polymide resin on a second (back) surface of a semiconductor element, as would be necessary to meet the features of claim 12. In particular, the Hashimoto Patent merely discloses in Fig. 10 resin layer 134 as a first underlying layer on an upper or first surface of wafer 130 that includes circuit

elements. Resin layer 134 of the Hashimoto Patent is not on a second surface of wafer 130. Moreover, there would be absolutely no reason or motivation to provide resin layer 134 in Fig. 10 of the Hashimoto Patent as peelably removable, because resin layer 134 is a permanent underlayer that remains on the upper surface of the wafer 130, and that has various wiring layers thereon.

The Examiner has asserted at the bottom of page 5 of the current Office Action that resin layer 134 of the Hashimoto reference (WO 98-25297) ***"may be formed by either sticking an adhesive tape or spin coating"***. The Examiner has alleged that although both processes may be used, the layer is preferably formed from an adhesive tape to avoid wasting resin material.

As noted above, the Hashimoto reference (WO 98-25297) is a non-English language document. Accordingly, the Examiner's assertion that resin layer 134 in Fig. 10 of the Hashimoto reference can be formed from an adhesive tape cannot be confirmed.

On the other hand, the Hashimoto Patent (USP 6,475,896) describes beginning in column 8, line 66 with respect to Fig. 1A, that wafer 10 may include resin layer 14 on an upper surface thereof, as formed by a spin coating method. As an alternative to a spin coating method, a pump may be used to eject ***"a tape-shaped polymide resin"***, to avoid wasting large quantities of polymide resin.

Applicant respectfully submits that the Hashimoto Patent does not describe that resin layer 14 (134) is formed by sticking an adhesive tape, or formed from an adhesive

tape, as alleged by the Examiner. That is, resin layer 14 (134) of the Hashimoto Patent is formed as being **ejected from a pump** as tape-shaped. The Examiner has clearly misconstrued the Hashimoto reference.

The secondarily relied upon Yamada reference teaches in column 1, lines 27-39 that to prevent damaging a semiconductor wafer from cracking at the time of grinding, it is commonly practiced to protect the front surface of the wafer where the semiconductor devices are formed, by an adhesive medium such as an adhesive tape. The Yamada reference does not disclose a protective layer that is a peelably removable UV sensitive tape made of a polymide resin on a second or back surface of a semiconductor element, as would be necessary to meet the features of claim 12.

The Kim et al. reference describes a chip protection layer 82 as formed by spin-coating a polymer such as polymide and epoxy on a back surface of a wafer, as shown in Fig. 23 and 24. The Kim et al. reference does not disclose a protective layer that is a peelably removable UV sensitive tape made by polymide resin, on a second surface of a semiconductor element, as would be necessary to meet the features of claim 12.

Accordingly, the prior art as relied upon by the Examiner taken together does not disclose the use of a peelably removable UV sensitive tape made of polymide resin on a second surface of a semiconductor element, and thus does not make obvious the features of claim 12. Applicant thus respectfully submits that the semiconductor device of claim 12 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 12 and 15, is

improper for at least these reasons.

The semiconductor device of independent claim 17 includes in combination among other features a protective layer "made of polymide resin on the second surface of the semiconductor element,...wherein the protective layer is a peelably removable UV sensitive tape which comprises a hardened synthetic resin that bonds the tape to the second surface of the semiconductor element". Independent claims 22 and 27 respectively include similar features. Applicant respectfully submit that the semiconductor devices of respective claims 17, 22 and 27 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 17, 20, 22, 25, 27 and 30 is improper for at least somewhat similar reasons as set forth above with respect to claim 12.

Claims 12, 15-17, 20-22, 25-27, 30 and 31 have been rejected under 35 U.S.C. 103(e) as being unpatentable over Applicant's admitted prior art (AAPA) in view of the Elenius et al., Kim et al., Hashimoto and Yamada references. Applicant respectfully submits that Applicant's admitted prior art Fig. 4 does not include a peelable UV tape on a back surface thereof, and thus would provide no motivation to modify the previously relied upon prior art to includes such features. Applicant's admitted prior art thus does not overcome the above noted deficiencies of the previously relied upon Elenius et al., Kim et al., Hashimoto and Yamada references. Accordingly, Applicant respectfully submits that this rejection is improper for at least these reasons.